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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/933,603	BERG ET AL.
	Examiner	Art Unit
	Joseph Manoskey	2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,8,11-17 and 20-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5,8,11-17 and 20-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2, 4, 5, 20, 24, 25, 27, 29, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim, U.S. Patent 4,371,930.

3. Referring to claim 27, Kim teaches a method for error detection and correction, this is interpreted as a memory error management method (See Col. 1, lines 15-20). Kim discloses reading from the memory that has check bits into a single-bit error detector and corrector, this is interpreted as reading information from an error checking and correction memory at a location (See Col. 3, lines 42-45 and 54-58). Next Kim teaches determining if the error is single bit error and correctable or a multiple bit error and uncorrectable, and if it is a single bit error correcting it, this is interpreted as if a correctable error exists in the information, correcting the error in the information (See Col. 1, lines 57-60 and Col. 4, lines 64-66). Finally Kim teaches restoring the correct word back into the same memory address and retrying to read to determine if it has been corrected, this is interpreted as rewriting the corrected information back into the

memory at the location and rereading information from the error checking and correction memory a the location to determine whether the correctable error has been corrected (See Col. 1, lines 57-68 and Col. 3, lines 54-58).

4. Referring to claim 2, Kim teaches the method using an error register to hold the information, this is interpreted as the information is a plurality of bits in a memory controller buffer cell (See Fig. 3, and Col. 4, lines 44-46).

5. Referring to claim 4, Kim teaches the method correcting single bit errors (See Col. 4, lines 64-66).

6. Referring to claim 5, Kim discloses the error correction code being hamming codes (See Col. 3, lines 45-49).

7. Referring to claim 29, Kim teaches a memory controller with a buffer (See Fig. 3, and Col. 4, lines 44-46). Kim discloses reading from the memory that has check bits into a single-bit error detector and corrector, this is interpreted as a reader that reads information from the memory controller buffer at a location (See Col. 3, lines 42-45 and 54-58). Next Kim teaches determining if the error is single bit error and correctable or a multiple bit error and uncorrectable, and if it is a single bit error correcting it, this is interpreted as an error detector that responds to information by determining whether a correctable error exists and a soft error corrector that cooperates with the error detector

by correcting the correctable error in the information (See Col. 1, lines 57-60 and Col. 4, lines 64-66). Finally Kim teaches restoring the correct word back into the same memory address and retrying to read to determine if it has been corrected, this is interpreted as a memory refresher that writes the corrected information back into the memory at the location and a checker that cooperates with the memory refresher to cause the reader to read information from the memory controller buffer at the location to determine whether the correctable error has been corrected (See Col. 1, lines 57-68 and Col. 3, lines 54-58).

8. Referring to claim 30, Kim discloses a process for correcting errors that detected in memory, this is interpreted as a memory error resolution process operable in a memory in which an error has been discovered in information stored in a memory location (See Col. 1, lines 15-20). Next Kim teaches determining if the error is single bit error and correctable or a multiple bit error and uncorrectable, and if it is a single bit error correcting it and Kim teaches restoring the correct word back into the same memory address and retrying to read to determine if it has been corrected, this is interpreted if a correctable error exists in the information, correcting the error in the information, rewriting the corrected information back into the memory at the location and rereading information from the error checking and correction memory at the location to determine whether the correctable error has been corrected (See Col. 1, lines 57-68, Col. 3, lines 54-58, and Col. 4, lines 64-66). Finally Kim discloses detecting whether the error is non-correctable because it is a multi-bit error or a solid, or "hard", single bit

error. In the first case Kim provides a multi-bit error signal and with the hard single bit error Kim logs the error, this is interpreted as if a non-correctable error exists in the information, performing a non-correctable error process (See Col. 3, lines 13-19 and Col. 5, lines 13-23).

9. Referring to claim 20, Kim teaches restoring the corrected error back into the memory, this is interpreted as a soft correctable error handling process is engaged if it is determined that the correctable error has been corrected (See Col. 3, lines 54-58).

10. Referring to claim 24, Kim teaches retrying the read to determine if the error has been corrected, this is interpreted as a recursive error handling process (See Col. 1, lines 57-68).

11. Referring to claim 25, Kim teaches determining if the error is a multi-bit error and thus cannot be corrected and causing a failure, this is interpreted as a predictive failure analysis process (See Col. 5, lines 13-23).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3, 8, 13, 14, 15, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Idleman et al., U.S. Patent 6,154,850, hereinafter referred to as "Idleman".

14. Referring to claim 3, Kim teaches all the limitations (See rejection of claim 27) except for the memory controller buffer being for a disk array memory system Idleman discloses dual memory controllers a disk array (See Fig. 3 and Col. 1, lines 11-16). It would be obvious to one of ordinary skill in the art at the time of the invention to use the memory controller that contains a buffer of Kim for the disk arrays of Idleman. This would have been obvious to one of ordinary skill in the art at the time of the invention because it memory controllers provide a method for interfacing a computer to a set of storage devices such as disks (See Col. 1, lines 4-10).

15. Referring to claim 8, Kim discloses all the limitations (See rejection of claim 27) except for the failover of the memory controller to an alternate memory controller to take responsibility of memory operations, however Kim does teach correcting errors that occur with system (See Col. 1, lines 15-29). Idleman discloses a system with dual controllers where one is the primary and the other acts as a backup (See Fig. 3 and Col. 3, lines 1-3). It would be obvious to one of ordinary skill in the art at the time of the invention to use the dual controller method of Idleman with memory controllers of Kim. This would have been obvious to one ordinary skill in the art at the time of the invention

to do because if one controller should fail the other will take control with out the computer getting involved (See Idleman, Col. 4, lines 42-48).

16. Referring to claims 13 and 15, Kim discloses all the limitations (See rejection of claim 29) except for the failover of the memory controller to an alternate memory controller to take responsibility of memory operations, however Kim does teach correcting errors that occur with system (See Col. 1, lines 15-29). Idleman discloses a system with dual controllers where one is the primary and the other acts as a backup (See Fig. 3 and Col. 3, lines 1-3). Idleman teaches a controller failing, this is interpreted as the input/output operation being not complete, and another controller acting as backup for the primary controller, this is interpreted as the alternate memory controller completing the input/output operation of the first controller (See Idleman, Col.3, lines 1-3 and Col. 4, lines 42-48). It would be obvious to one of ordinary skill in the art at the time of the invention to use the dual controller method of Idleman with memory controllers of Kim. This would have been obvious to one ordinary skill in the art at the time of the invention to do because if one controller should fail the other will take control with out the computer getting involved (See Idleman, Col. 4, lines 42-48).

~~17. Referring to claim 14, Kim and Idleman teach all the limitations (See rejection of claim 13) including a controller failing, this is interpreted as the input/output operation being not complete, and another controller acting as backup for the primary controller,~~

this is interpreted as the alternate memory controller completing the input/output operation of the first controller (See Idleman, Col.3, lines 1-3 and Col. 4, lines 42-48).

18. Referring to claim 22, Kim discloses all the limitations (See rejection of claim 30) except for the failover of the memory controller to an alternate memory controller to take responsibility of memory operations, however Kim does teach correcting errors that occur with system (See Col. 1, lines 15-29). Idleman discloses a system with dual controllers where one is the primary and the other acts as a backup (See Fig. 3 and Col. 3, lines 1-3). Idleman teaches a controller failing, this is interpreted hard fault, and another controller acting as backup for the primary controller, this is interpreted as correcting a hard fault (See Idleman, Col.3, lines 1-3 and Col. 4, lines 42-48). It would be obvious to one of ordinary skill in the art at the time of the invention to use the dual controller method of Idleman with memory controllers of Kim. This would have been obvious to one ordinary skill in the art at the time of the invention to do because if one controller should fail the other will take control with out the computer getting involved (See Idleman, Col. 4, lines 42-48).

19. Referring to claim 23, Kim discloses all the limitations (See rejection of claim 30) except for the failover of the memory controller to an alternate memory controller to take responsibility of memory operations, however Kim does teach correcting errors that occur with system (See Col. 1, lines 15-29). Idleman discloses a system with dual controllers where one is the primary and the other acts as a backup (See Fig. 3 and Col.

3, lines 1-3). Idleman teaches a controller failing, this is interpreted as the input/output operation being not complete, and another controller acting as backup for the primary controller, this is interpreted as the alternate memory controller completing the input/output operation of the first controller (See Idleman, Col.3, lines 1-3 and Col. 4, lines 42-48). It would be obvious to one of ordinary skill in the art at the time of the invention to use the dual controller method of Idleman with memory controllers of Kim. This would have been obvious to one ordinary skill in the art at the time of the invention to do because if one controller should fail the other will take control with out the computer getting involved (See Idleman, Col. 4, lines 42-48).

20. Claims 11, 12, 26, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Beffa et al., U.S. Patent 6,477,662, hereinafter referred to as "Beffa".

21. Referring to claims 11 and 12, Kim discloses all the limitations (See rejection of claim 29) except for the controller fencing off a location of the error in the buffer, however Kim does teach having solid uncorrectable errors in memory (See Col. 2, lines 54-60). Beffa teaches isolating defective locations in memory, or buffer, called "partialing", this is interpreted as fencing off a location (See Col. 7, lines 18-27). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the error location in the buffer of Kim with the "partialing" of Beffa to force a rewrite to a new location in the buffer. This would have been obvious to one of ordinary

skill in the art at the time of the invention to do because it allows a memory with defective cells to still be used (See Beffa, lines 25-27).

22. Referring to claims 26 and 28, Kim discloses all the limitations (See rejection of claims 30 and 27 respectively) except for the controller fencing off a location of the error in the memory, however Kim does teach having solid uncorrectable errors in memory (See Col. 2, lines 54-60). Beffa teaches isolating defective locations in memory, called "partialing", this is interpreted as fencing off a location (See Col. 7, lines 18-27). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the error location in the memory of Kim with the "partialing" of Beffa to force a rewrite to a new location in the memory. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows a memory with defective cells to still be used (See Beffa, lines 25-27).

23. Claims 16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Kiyonaga et al., U.S. Patent 5,371,745, hereinafter referred as "Kiyonaga".

24. Referring to claim 16, Kim teaches all the limitations (See the rejection of claim 29) except for the soft error corrector comprising an XOR array and an accumulator for storing information associated with the logic and arithmetic operations of the XOR array, said accumulator coupled to said XOR array. Kiyonaga discloses the memory controller

having error correction circuitry using parity, which is interpreted as being an XOR array for providing correction to single bit errors (See Fig. 3, Col. 7, lines 39-41). Kiyonaga also discloses a retry counter for counting the number of retries, this is interpreted as the memory controller having an accumulator for storing information associated with operations of the XOR array (See Fig. 3 and Col. 8, lines 35-45). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the soft error corrector of Kim with XOR array and accumulator of Kiyonaga. This would have been obvious to do because it provides a counter to determine the number of retries (See Col. 8, lines 35-35).

25. Referring to claim 21, Kim teaches all the limitations (See rejection of claim 20) except for including a soft error correctable count, however Kim does teach logging errors (See Col. 3, lines 13-19). Kiyonaga teaches the using a retry counter for counting retries, this is interpreted as incrementing a soft-error correctable error count for a soft correctable error handling process (See Col. 8, lines 35-45). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine logging of errors of Kim and Idleman with the counting of errors of Kiyonaga. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it provides a counter to determine the number of retries (See Col. 8, lines 35-35).

26. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim and Idleman in view of Kiyonaga.

27. Referring to claim 17, Kim and Idleman teach all the limitations (See the rejection of claim 13) except for tracking of error information that includes counts of soft, hard and non-correctable errors, however Kim does teach logging errors (See Col. 3, lines 13-19). Kiyonaga teaches a retry counter in the controller that keeps count of errors and the number of times data correction was repeated, this is interpreted as the processing core keeping track of error information including counts of soft, hard, and non-correctable errors (See Fig. 3, and Col. 8, lines 35-45). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine logging of errors of Kim and Idleman with the counting of errors of Kiyonaga. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it provides a counter to determine the number of retries (See Col. 8, lines 35-35).

Response to Arguments

28. Applicant's arguments, see page 8 of amendment, filed 02 August 2004, with respect to the drawings have been fully considered and are persuasive. The objection of the drawings has been withdrawn.

29. Applicant's arguments, see page 8 of amendment, filed 02 August 2004, with respect to claim 22 have been fully considered and are persuasive. The objection of claim 22 has been withdrawn.

30. Applicant's arguments, see page 8 of amendment, filed 02 August 2004, with respect to claims17 and 20 have been fully considered and are persuasive. The 35 U.S.C. 112 rejections of claims 17 and 20 have been withdrawn.

31. Applicant's arguments, see page 8-13 of amendment, filed 02 August 2004, with respect to the rejection(s)of claim(s) 1-26 under 35 U.S.C. 102(b) and 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection for the now amended claims 2-5, 8, 11-17, and 20-30, is made in view of Kim. See above rejection.

Conclusion

32. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. After approximately October 13, the examiner can be reached at the new Alexandria telephone number, (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
October 8, 2004

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